Application No. 10/065, 005
Amendment dated July 22, 2005
Amendment made in response to Office Action dated April 05, 2005

Amendments to the Claims

This listing of claims will replace all prior versions and listing of claims in the application:

Listings of Claims:

1. (currently amended) An interface unit for communication between an integrated services digital network (ISDN) based bus and a processor bus, wherein data in the ISDN-based bus is transferred in ISDN frames divided into a plurality of slots comprising:

a data transfer unit includes

a processor bus interface coupled to a processor bus, the processor bus interface includes a processor buffer,

an ISDN bus interface coupled to an ISDN-based bus, the ISDN bus interface includes an ISDN buffer;~~,~~ and

a control unit coupled to the data transfer unit for controlling the transfer of data between the processor bus and ISDN-based bus,

wherein the interface unit facilitates communication between a device coupled to the ISDN bus and a device coupled to the processor bus, the interface unit is capable of accessing all slots in an ISDN frame.

2. (original) The interface unit of claim 1 wherein said processor bus interface is coupled to the ISDN-ba sed bus interface via an interface buffer comprising a group of register banks, said group of register banks having a control input terminal.

3. (original) The interface unit of claim 2 wherein the control unit further comprises a register bank control unit coupled to the interface buffer for controlling the group of register banks.

4. (original) The interface unit of claim 1 wherein the ISDN buffer comprises at least one shift register for parallel/serial data conversion.

5. (original) The interface unit of claim 1 wherein the processor bus interconnects a central processing unit, a memory unit and peripheral devices.

6. (original) The interface unit of claim 5 wherein the ISDN-based bus comprises an ISDN-oriented modular bus for coupling to voice, data and/or video devices.

7. (original) The interface unit of claim 1 wherein said processor bus is connected to a high-speed data transfer unit.

8. (original) The interface unit of claim 7 wherein the high-speed data transfer unit is a Universal Serial Bus.

9. (currently amended) An interface to facilitate communication between an ISDN-based bus which communicates in ISDN frames divided into a plurality of slots and a processor bus comprising:

a data transfer unit for buffering data that are to be transferred between a device coupled to the processor bus and a device on the ISDN-based bus ; and

a control unit coupled to the data transfer unit for controlling the transfer of data between the device coupled to the processor bus and the device coupled to the ISDN-based bus, wherein the interface is capable of accessing all slots of an ISDN frame.

10. (previously presented) The interface of claim 9 wherein the control unit is programmed to determine the direction of data transfer and which slot or slots to access.

11. (previously presented) The interface of claim 10 either operates in frame-based processing or in slot-based processing.

12. (previously presented) The interface of claim 10 wherein the data transfer unit comprises a memory module for buffering data that are to be transferred between the processor bus and the ISDN-based bus.

13. (previously presented) The interface of claim 12 either operates in frame-based processing or in slot-based processing.

14. (previously presented) The interface of claim 9 wherein the data transfer unit comprises a memory module for buffering data that are to be transferred between the processor bus and the ISDN-based bus.

15. (previously presented) The interface of claim 14 either operates in frame-based processing or in slot-based processing.

16. (previously presented) The interface of claim 9 either operates in frame-based processing or in slot-based processing.

17. (previously presented) The interface of claim 9 wherein the data transfer unit comprises:

processor bus interface storage (PBIS) block coupled to the processor bus, wherein the PBIS includes a PBIS memory unit for buffering data that are to be transferred to or received from the processor bus; and

ISDN-based bus interface storage (IBIS) block coupled to the ISDN-based bus, wherein the IBIS includes an IBIS memory unit for storing data that are to be transferred to or received from the ISDN-based bus.

18. (previously presented) The interface of claim 17 wherein the control unit comprises a control register block (CRB) coupled to the processor bus for receiving control information for

programming the interface, wherein based on the information, the appropriate port, time slots and direction are selected for data transfer.

19. (previously presented) The interface of claim 17 wherein the data transfer unit further comprises an interface buffer (IB) coupled to the PBIS and IBIS, the IB provides intermediate buffering of data between the PBIS and IBIS blocks.

20. (previously presented) The interface of claim 19 wherein the IB comprises a plurality of register banks, each register bank comprising a plurality of registers to form a register stack.

21 (previously presented) The interface of claim 19 wherein the IB includes first and